Remarks

In the non-final Office Action dated May 14, 2009, the following new grounds of rejection were indicated: claims 1, 2, 5, 6, 14-16 and 21 were rejected under 35 U.S.C. § 103(a) over Krishnamurthy (U.S. Patent No. 6,233,178) in view of Iwahashi (U.S. Patent No. 4,247,918); claims 3, 7-9, 11, 17 and 20 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 reference further in view of Guliani (U.S. Patent No. 6,366,497); claims 4 and 10 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918 and '497 references and further in view of Takahashi (U.S. Patent No. 6,639,849); and claims 12-13 and 18-20 were rejected under 35 U.S.C. § 103(a) over the '178 reference in view of the '918, '497 and '849 references and further in view of Kurihara (U.S. Patent Pub. 6,791,880). Applicant respectfully traverses all claim rejections, and in this discussion set forth below, does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the § 103(a) rejections because the '178 reference is directed to a different type of memory from the claimed invention (*i.e.,* floating gate instead of charge trapping) and teaches away from the proposed modification. The floating gate memory of the '178 reference is susceptible to overcharging whereas the charge trapping of the claimed invention is susceptible to over discharging, which is addressed by Applicant via a preconditioning step that charges the memory devices before performing a block erase that discharges the memory devices. The Office Action proposes to modify the '178 reference to precondition its floating gate memory by charging; however, such a modification is improper because the '178 reference expressly teaches away from charging already charged memory cells and because Applicant's disclosure is the only art of record that teaches or suggests the desirability of preconditioning by charging. The following discussion particularly addresses the impropriates of the § 103(a) rejections.

Applicant appreciates the Office Action's attempt to address Applicant's prior arguments, however, Applicant respectfully submits that the newly applied rejections confuse logical values of '1' and '0' with physical charge states. While a physical charged state can be interpreted as either a logical '0' or a '1', the physical charge state of

flash memory remains the same. Thus, the required erasure and programming step for a write operation does not change simply because the logical values are swapped. Accordingly, the proposed modification would not correspond to the claim limitations.

The Office Action also fails to consider the fact that the '178 reference relates to floating gate memory, whereas Applicant's claimed invention is directed towards charge trapping memories. In this respect, Applicant's specification explains that the inventor observed that charge trapping memories exhibit different characteristics from floating gate memories (*see, e.g.*, Applicant's specification, page 2:16-20), and that 'program induced degradation' does not exist for charge trapping memory devices (*see, e.g.*, Applicant's specification, page 15:28-16:5). In contrast, the '178 reference expressly teaches that the problem being addressed by the '178 reference is due to excess charge buildup. Thus, the proposed combination, based upon the primary '178 reference, not only fails to correspond to the claim limitations but also expressly teaches that charging is a problem to be avoided. Since Applicant's specification is the only art of record that explains and teaches that charging of charge trapping memory devices is beneficial, it is impermissible for the Office Action to allege obviousness of this recognition especially where the cited references expressly lead the skilled artisan in the opposite direction. This is supported by numerous rules and legal holdings, some of which are explained in more detail hereafter.

The stated purpose of the '178 reference is to precondition the cells before an erasure ever occurs to specifically avoid charging an already charged cell. The '178 reference explains that this is done to mitigate stress build up due to erasures (Col. 5:39-40). The Examiner's proposed modification of the '178 reference would result in charging already charged cells. As such, it is impermissible to modify the '178 reference in a manner that defeats the express and primary purpose of avoiding charging already charged cells. "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." M.P.E.P. 2143.01 citing *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As consistent with the above, the '178 reference also teaches away from the claimed invention. The discharging and subsequent charging steps of the '178 reference

are described in the reference's Abstract and cited column 4, in which flash memory devices are first preconditioned by discharging cells, prior to charging the cells. The erasing step in the '178 reference is further described at column 5:1-3, which indicates that "[d]uring the erase step 320, all cells 120 within a sector are erased, setting cells 120 within the sector to their charged state" (*i.e.*, the cells are erased by charging). This is consistent with the discussion at page 3 of the Office Action, which states that the '178 reference "discharges cells as taught in Col 4 lines 43-45" as a preconditioning (first) step.

Importantly, the background of Applicant's specification explains, according to the teachings of the '178 reference, various issues with the reference's charging and discharging approach (see paragraphs 0006 and 0007 of the Background of the instant application). Specifically, the '178 reference's preconditioning step involves discharging that may result in discharging an already discharged memory cell, which can deteriorate the cell. The claimed invention addresses such problems (*see*, *e.g.*, paragraph 0008) and presents a memory control solution with results that are clearly different than those in the '178 reference. Accordingly, since the '178 reference teaches a memory management approach that causes the problems noted in the background of the instant application, the reference actually teaches away from the asserted combination of references.

The M.P.E.P. and the applicable U.S. Supreme Court law requires that the claim be considered "as a whole" (35 U.S.C. §103(a)), while taking into consideration the problem(s) being addressed by the claimed invention and any unexpected results. Thus, the Supreme Court in *KSR* reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), and stated that, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." The Court further tied in the relationship between the teach-away standard and demonstrating unpredictable results. "The fact that the elements [in *Adams*] worked together in an unexpected and fruitful manner supported the conclusion that Adam's design was not obvious to those skilled in the art." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007). Accordingly, the '178 reference not only fails to disclose or contemplate the claimed invention, it further teaches away from the claimed invention.

In view of the above, the cited portions of the '178 reference fail to disclose, teach or suggest limitations in both of independent claims 1 and 5. As the rejections of claims 2-15 and 21 rely upon the misapplied portions of the '178 reference, these rejections are improper and should be removed.

In view of the above, Applicant believes that further discussion of the Section 103 rejections is unnecessary. However, Applicant submits that the proposed combinations of references cannot stand, as the resulting structure would not correspond to the claimed invention (per the above), and would render the '178 reference inoperable for its purpose (as relevant to replacing its discharging/charging steps with the steps as claimed), which contradicts the M.P.E.P. and relevant law. Applicant therefore submits that the Section 103 rejections are also improper for these reasons. Notwithstanding, Applicant has introduced facilitating amendments directed toward programming in response to a block erase request. As explained throughout Applicant's specification, the block programming step (*e.g.*, FIG. 5, 51) is implemented as part of a sector erase action (*e.g.*, FIG. 5, 56). Accordingly, the amendments are fully supported and are believed to be consistent with aspects implicit in the previous claims.

Applicant further notes that the rejection of claims 8 and 17 does not establish a *prima facie* case of obviousness. The cited portion of the '497 reference simply teaches that the reference cell can be used for programming or erasing configurations, but it does not teach that the reference cell is actually programmed and erased for a block-programming and block-erasing of the non-volatile memory devices in the array. Applicant directs the Examiner to Applicant's specification beginning at page 17, which explains the differences between floating gate memories and charge trapping memories and provides evidence of the nonobviousness of this aspect (*e.g.*, due to aspects taught by Applicant's specification and not otherwise recognized by the references cited in the rejection of claims 8 and 17).

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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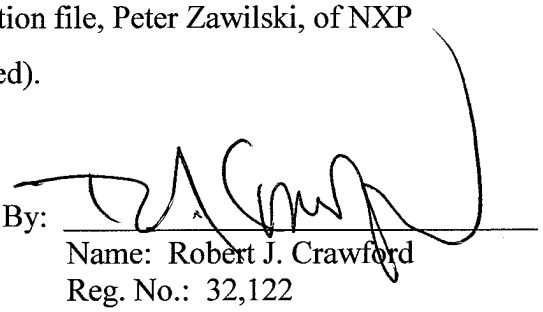
By: 

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